ECSE 222 – DIGITAL LOGIC

VHDL ASSIGNMENT 2

LAB REPORT

Group:

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# SUMMARY

In this assignment, we learnt to create a schematic gate diagram of a logic circuit using CAD tools on Quartus Prime, as well as write VHDL testbench based on the template file. We then synthesize the logic circuit/function and perform the simulation on ModelSim. (must paraphrase bc of plagiarism)

# QUESTIONS

# FIGURES

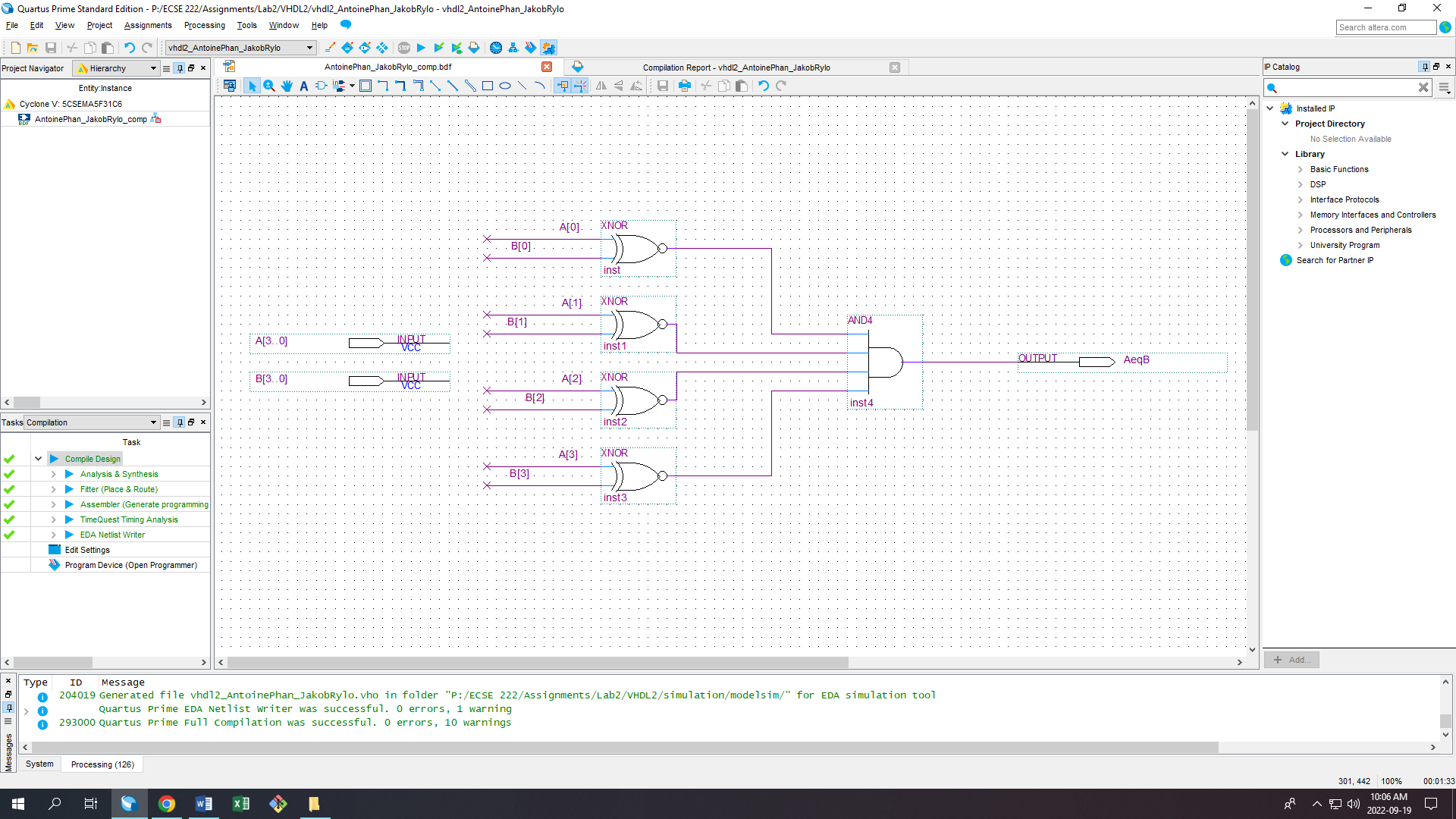


Figure 1: Schematic diagram design of the circuit

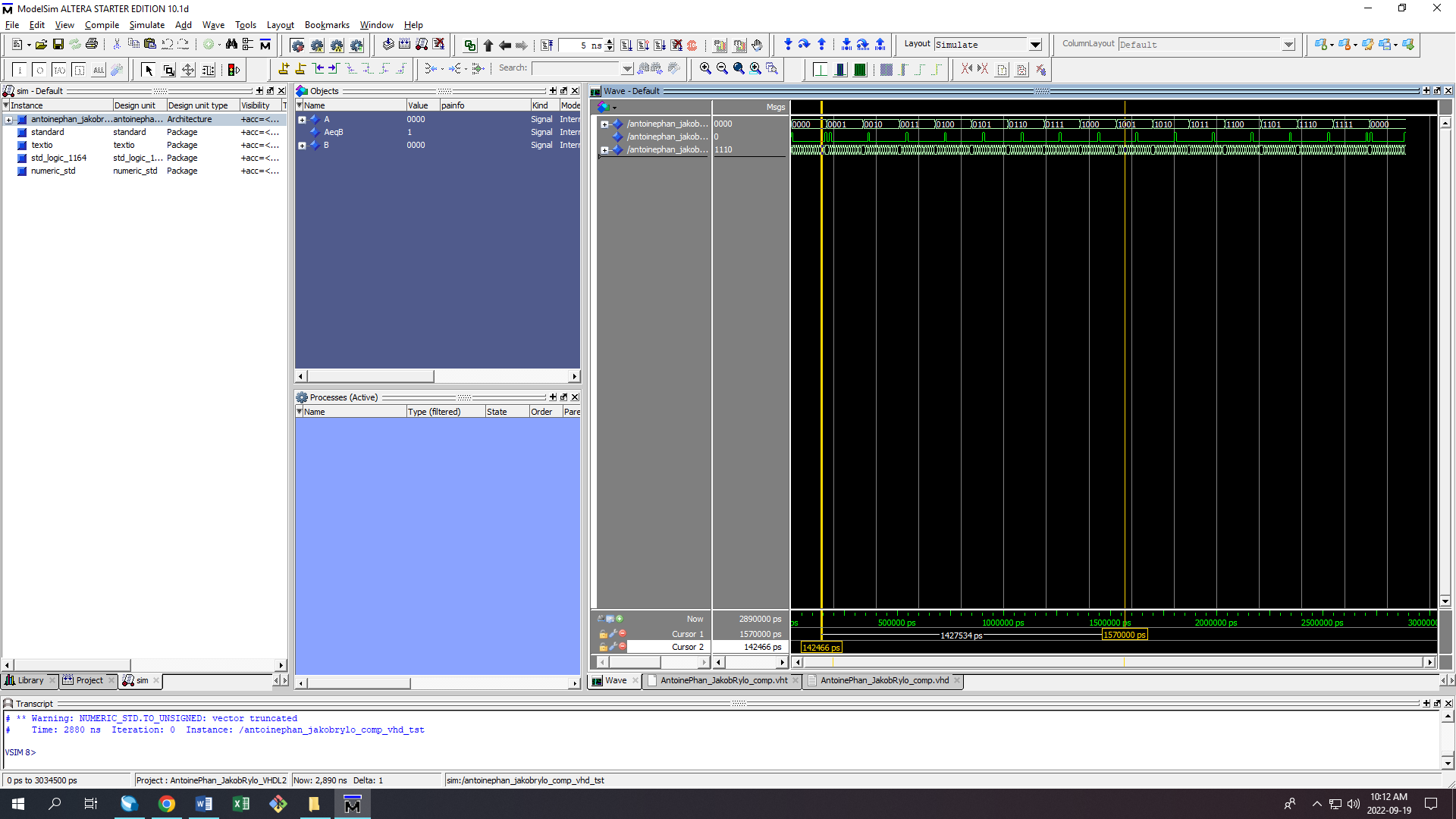


Figure 2.1: Simulation of the schematic diagram design (brute force)

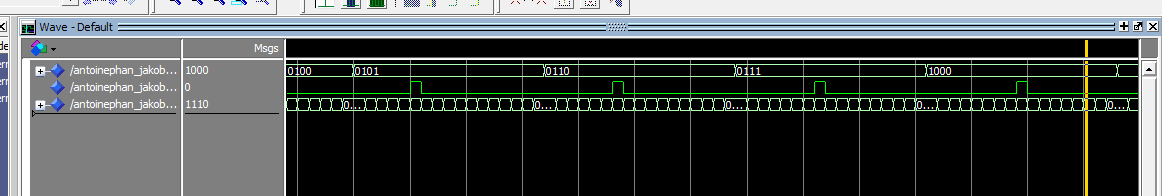


Figure 2.2: A close-up zoom-in of the simulation on ModelSim

# EXPLANATION

# CONCLUSION